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Semiconductor Processing Methods, Methods Of Forming Electronic Components, And Transistors

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TECHNICAL FIELD

This invention relates to semiconductor processing methods, including methods of fabricating electronic components such as transistors.

BACKGROUND OF THE INVENTION

Field effect transistors are comprised of a pair of diffusion regions, referred to as a source and a drain, spaced apart within a semiconductive substrate. The transistors include a gate provided adjacent a substrate separation region between the diffusion regions for imparting an electric field to enable current to flow between the diffusion regions. The substrate material adjacent the gate and between the diffusion regions is referred to as the channel.

The semiconductive substrate typically comprises bulk crystalline silicon having a light conductivity doping impurity concentration of opposite type to the predominate doping of the source and drain regions. Alternately, the substrate can be provided in the form of a thin layer of lightly doped semiconductive material over an underlaying insulating layer. Such are commonly referred to as semiconductor-on-insulator (SOI) constructions. In the context of this document, the term "semiconductive substrate" is defined to mean any

construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Integrated circuitry fabrication technology continues to strive to increase circuit density, and thereby minimize the size and channel lengths of field effect transistors. Improvements in technology have resulted in reduction of field effect transistor size from long-channel devices (i.e., channel lengths greater than two microns), to short-channel devices (i.e., channel lengths less than two microns), and to sub-micron devices (i.e., channel lengths less than one micron). As field effect transistor channel lengths (i.e., gate or word line widths) became smaller than two microns, so-called short-channel effects began to become increasingly significant. As a result, device design and consequently process technology had to be modified to take these effects into account so that optimum device performance could continue to be obtained. For example, the lateral electrical field in the channel region increases as a result of smaller transistor channel lengths as the supply voltage remains constant. If the field becomes strong enough, it can give rise to so-called hot-carrier effects. Hot-carrier effects often lead to gate

oxide degradation, as energetic carriers can be injected into gate oxide and become permanent charges.

Two recognized solutions to this problem, used either alone or in combination, include source/drain re-oxidation and provision of lightly doped drain (LDD) regions. Source/drain re-oxidation effectively grows a layer of thermal oxide over the source and drain areas as well as over the gate sidewalls. The oxidation has the effect of rounding the poly gate edge corners in effectively oxidizing a portion of the gate and underlying substrate, thereby increasing the thickness of the gate oxide layer at least at the edges of the gate. Such reduces the gate-to-drain overlap capacitance, and strengthens the gate oxide of the polysilicon gate edge. The latter benefits are effectively obtained because oxidation-induced encroachment gives rise to a graded gate oxide under the polysilicon edge. The thicker oxide at the gate edge relieves the electric-field intensity at the corner of the gate structure, thus reducing short-channel effects.

An example technique for accomplishing such re-oxidation includes conventional wet and dry oxidations at atmospheric pressure and at a temperature of 800°C or greater. Typical process exposure time is 10 minutes, which also grows a layer of oxide from 50 to 200 Angstroms thick on the sidewalls of the patterned gate.

LDD regions are provided within the substrate relative to the channel region in advance of the source and drains, and further reduce hot-carrier effects. The LDD regions are provided to be lighter

conductively doped (i.e., less concentration) than the source and drain regions. This facilitates sharing the voltage drop between the drain and the channel, as opposed to the stark voltage drop at the channel occurring in non-LDD transistors. The LDD regions absorb some of the voltage drop potential into the drain, thus effectively eliminating hot-carrier effects. As a result, the stability of the device is increased.

Most commonly, a combination of source/drain re-oxidation and formation of LDD regions is utilized. However in combination, these processes can create problems, particularly in fabrication of sub-micron devices.

For example, consider Figs. 1-2. Fig. 1 depicts a semiconductor wafer fragment 10 comprised of a bulk monocrystalline substrate 12 having a gate structure 14 formed thereover. Gate 14 comprises a gate oxide layer 16, an overlying conductively doped polysilicon layer 18, an overlying refractory metal silicide layer 20, and an insulative cap 22, such as Si_3N_4. That region beneath gate oxide layer 16 within bulk substrate 12 will constitute the channel region of the resultant transistor. Unfortunately when subjected to source/drain re-oxidation, the differing materials of gate 14 do not oxidize at the same rate. Fig. 2 illustrates an oxide layer 24 formed over substrate 12 and the sidewalls of gate structure 14 after a source/drain re-oxidation. Silicide layer 20 of gate structure 14 has a tendency to oxidize at a significantly greater rate than the oxidation of either nitride layer 22 or polysilicon layer 18. Such results in the formation of the illustrated sidewall bulges 25.

The typical manner by which LDD regions are fabricated is by ion implantation of conductivity dopant impurity after source/drain re-oxidation, such as regions 26. Unfortunately, oxide bulges 25 in layer 24 effectively function as a mask to such ion implantation. This results in formation of LDD implant regions 26 being laterally spaced outwardly away from the original sidewalls of gate structure 14. This is undesirable. More preferably, the inner lateral edges of LDD regions 26 are desirably as close to the gate edges as possible.

The invention was principally motivated in overcoming drawbacks such as that described above with respect to field effective transistors fabrication. The artisan will, however, appreciate applicability of the following invention to other aspects of semiconductor wafer processing in formation of other electronic components or devices, with the invention only being limited by the accompanying claims appropriately interpreted in accordance with the Doctrine of Equivalents.

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SUMMARY OF THE INVENTION

The invention comprises semiconductor processing methods, methods of forming electronic components, and transistors. In one implementation, first and second layers are formed over a substrate. One of the layers has a higher oxidation rate than the other when exposed to an oxidizing atmosphere. The substrate has a periphery. The layers, respectively, have an exposed outer edge spaced inside the

substrate periphery. Etching is conducted into the higher oxidation rate material at a faster rate than any etching which occurs into the lower oxidation rate material. After the etching, the substrate is exposed to the oxidizing atmosphere.

In but one other implementation, a stack of at least two conductive layers for an electronic component is formed over a substrate. The two conductive layers have different oxidation rates when exposed to an oxidizing atmosphere. The layer with the higher oxidation rate has an outer lateral edge which is recessed inwardly of a corresponding outer lateral edge of the layer with the lower oxidation rate. The stack of conductive layers is exposed to the oxidizing atmosphere effective to grow an oxide layer over the outer lateral edges of the first and second layers.

In but one other implementation, a transistor comprises a semiconductive substrate and a gate stack formed thereover. The gate stack in at least one cross section defines a channel length within the semiconductive substrate of less than 1 micron, with the gate stack comprising conductive material formed over a gate dielectric layer. An insulative layer is formed on outer lateral edges of the conductive material, with the insulative layer having opposing substantially continuous straight linear outer lateral edges over all conductive material of the gate stack within the one cross section.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a prior art semiconductor wafer fragment at a prior art processing step, and is described in the "Background" section above.

Fig. 2 is a view of the Fig. 1 wafer fragment at a prior art processing step subsequent to that show by Fig. 1.

Fig. 3 is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 4 is a view of the Fig. 3 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 3 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a view of the Fig. 3 wafer fragment at a processing step subsequent to that shown by Fig. 5.

Fig. 7 is a view of the Fig. 3 wafer fragment at a processing step subsequent to that shown by Fig. 6.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring initially to Fig. 3, a semiconductor wafer fragment 30 comprises a bulk monocrystalline silicon substrate 32. A gate dielectric layer 33 (i.e., SiO_2), a conductively doped silicon layer 34 (i.e., polysilicon), a silicide layer 35 (i.e., a refractory metal silicide, such as WSi_x) and an insulating layer 36 (i.e., doped or undoped SiO_2, Si_3N_4, etc.) are formed over monocrystalline substrate 32. Silicide layer 35 has a higher oxidation rate than oxidation rates of layers 34 and 36 when exposed to an oxidizing atmosphere, with an example oxidizing atmosphere being oxygen gas at a temperature of about 950°C.

Referring to Fig. 4, insulating layer 36, silicide layer 35, doped silicon layer 34, and gate dielectric layer 33 are patterned and etched (i.e., by photolithography) to form a conductive gate stack 38 (having an insulating cap 39) over a channel region 40 of substrate 32. The preferred technique for forming the illustrated stack is by dry etching, for example, using chemistries comprising CH_4/CHF_3 for the insulative cap, NF_3/Cl_2 for the silicide, and Cl_2/HBr for the polysilicon. Gate stack 38 comprises two opposing and respectively linearly aligned outer lateral edges 42 and 44 of the insulating silicide and doped silicon layers. Accordingly or alternately considered, layers 34 and 35 constitute first and second layers (both being conductive in this example)

formed over a substrate, with the second layer being formed over the first and having a higher oxidation rate than the first when exposed to a certain oxidizing atmosphere. Although layer 35 is shown received over layer 34, the relationship might be reversed depending on the processor's desire and the component being fabricated. The first and second conductive materials in this example have been etched to form a conductive component, here in the form of a transistor gate 38. The substrate has a periphery (outside of the cross-sectional views of Figs. 3-7), with first layer 34 having an exposed first outer edge (i.e., either edge 42 or 44) spaced inside the substrate periphery, and with second layer 35 having an exposed first outer edge (i.e., either edge 42 or 44) spaced inside the substrate periphery.

Layer 36 (cap 39) comprises a third layer formed over the first and second layers, with itself having an exposed outer edge (i.e., either edge 42 or 44) spaced inside the substrate periphery. Third layer 36 has a lower oxidation rate than the oxidation rate of second layer 35 when exposed to the oxidizing atmosphere. The invention is believed to have its greatest applicability to electronic component device fabrication having widths less than 1 micron. Accordingly, the etching(s) to produce the Fig. 4 construction is ideally conducted to space opposing linear outer lateral edges 42 and 44 less than 1 micron apart from one another. Accordingly in the illustrated preferred embodiment where a transistor is being fabricated in the preferred sub-micron fabrication, the illustrated first conductive layer 34 is at least fabricated

to have its opposing outer lateral edges spaced less than 1 micron apart. Such defines, in the illustrated cross-section, a channel length (i.e., minimum gate width) within channel region 40 of semiconductive substrate 32 of less than 1 micron.

Referring to Fig. 5, silicide layer 35 is etched at a faster rate than any etching into edges 42 and 44 of layers 36 and 34 to recess outer lateral edges of silicide layer 35 to within outer lateral edges of both layers 36 and 34 of the illustrated stack. Such produces conductive layers 34 and 35 within the illustrated cross-section to have respective opposing outer lateral edges which are displaced from one another. Accordingly, the outer lateral edge of the layer with the higher oxidation rate is recessed inwardly of corresponding outer lateral edges of the layers with lower oxidation rate in the particular oxidizing atmosphere.

The preferred etching is a wet etching, preferably with a basic solution. An example is a solution comprising ammonium hydroxide and hydrogen peroxide, with a specific example solution being ammonium hydroxide, H_2O_2, and H_2O in a mix of 0.25:1:5 by volume. Example conditions for such etching include ambient pressure, a temperature ranging from 40°C to 70°C for from 1 to 10 minutes. Alternate bases (i.e., KOH) could be used in addition to or instead of ammonium hydroxide in the preferred basic wet etching. Such example chemistries can provide substantially selective etching of layer 35 relative to the etching of layers 36, 34, and substrate 32 if it is exposed. In the

context of this document, "substantially selective" is to be interpreted to mean an etch rate of one material relative to another of at least 2:1.

Referring to Fig. 6, the substrate is exposed to the oxidizing atmosphere with a recessed edge of second layer 35 being exposed. In the preferred embodiment, this is conducted to be effective to grow an oxide layer 50 over outer lateral edges of silicide layer 35 and doped silicon layer 34. Such is also effective to form oxide layer 50 over silicon substrate 32 and even, to perhaps a lesser degree, over insulating cap 39. Thus, a recessed edge of layer 35 is oxidized. Preferably, layer 50 is formed to produce oxide layer 50 to have opposing substantially continuous straight linear outer lateral edges 52 at least over first and second conductive materials 35 and 34 (i.e., over all conductive material of the gate stack within at least the one illustrated cross-section). Regardless and ideally, the prior art Fig. 2 outward lateral bulges 25 do not occur. Oxide layer 50 ideally has a lateral thickness of less than 100 Angstroms and greater than 10 Angstroms over first conductive material 34. Further ideally in the application of the invention to ever increasingly sub-micron devices, opposing linear outer lateral edges 52 of oxide layer 50 are formed to be less than 1 micron in separated distance. Alternate insulating material layers 50 could also of course be utilized.

After the preferred oxidizing to form oxide layer 50, a suitable dopant impurity is ion implanted into substrate 32 proximate gate stack 38 to form one or more LDD regions, or halo regions, 60.

Effective removal or prevention of formation of lateral bulges 25 of the Fig. 2 prior art can accordingly be utilized to position regions 60 more proximate the outer lateral edges of the gate stack, particularly in fabrication of sub-micron devices.

Referring to Fig. 7, insulative material is formed over oxide layer 50 and is subsequently anisotropically etched to produce insulative illustrated spacers 62. Subsequent ion implanting can then be conducted to provide dopant impurity into substrate 32 proximate the gate stack to form field effect transistor source/drain regions 64.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.